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NEW QUESTION: 1

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Answer: D

Explanation:

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NEW QUESTION: 2

Click and drag the memory type on the left to match it with its description on the right.

Answer:

Explanation:

Explanation:

* RDIMM

RDIMMs add a register, which buffers the address and command signals. The integrated memory controller in the CPU sees the register instead of addressing the memory chips directly.

* LRDIMM

Load Reduced DIMMs replace the register with an Isolation Memory Buffer (iMB by Inphi) component. The iMB buffers the Command, Address, and data signals. The iMB isolates all electrical loading (including the data signals) of the memory chips on the (LR)DIMM from the host memory controller.

* UDIMM

UDIMM (unregistered memory) is a type of memory chip used mostly in desktop and laptop computers. More commonly called unbuffered memory, UDIMMs run faster than registered memory (RDIMM) and cost less, but are not quite as stable as RDIMMs.

* NVDIMM

A Non-Volatile Dual In-line Memory Module (NVDIMM) is a computer memory RAM DIMM that retains data even when electrical power is removed either from an unexpected power loss, system crash or from a normal system shutdown. NVDIMMs can be used to improve application performance, data security, system crash recovery time and to enhance SSD endurance and reliability.

References:

<http://www.anandtech.com/show/6068/lrdimms-rdimms-supermicros-latest-twin/2>

NEW QUESTION: 3

Hotspot Question

Match each technology to its description.

Answer:

Explanation:

http://h71000.www7.hp.com/doc/83final/b9073_90111/apas13.html
The LPMC monitor, within the Support Tools Manager (STM) diagnostics, generates Information events for all cache errors that are detected. After three errors (Threshold) have been detected on a processor in 1440 minutes, or a 24-hour period of time (Period), the monitor deactivates that particular processor, marks it for deconfiguration on the next system reboot, and generates a SERIOUS event. After the failed processor is deactivated, the LPMC monitor attempts to activate one of the inactive Instant Capacity processors, if any are available. This method ensures the processing power of the system is unchanged.

A default value of "three" is assigned to Threshold, except for the PCX-W+ family of processors, which has a value of "five" assigned. The default value assigned to a Period is 1440 minutes, or 24 hours, in all possible processor configurations. An inactive processor under warranty or support automatically replaces a failed processor. HP also services and replaces any failed processor.

<http://www.techrepublic.com/whitepapers/mca-error-recovery-hp-ux-feature-for-recovering-frommachinecheck-aborts/354967>

HP Integrity servers provide superior reliability and availability. Nevertheless, even the best of computers can occasionally experience hardware problems that lead to unplanned downtime. Some of these problems are caused by transient events such as an alpha particle strike on memory, cache, or a processor data structure.

Intel Itanium-based servers support an advanced architecture that allows the system to contain, correct, and signal machine check errors. Many of these errors are corrected by the platform without operating system intervention. When the platform cannot correct an error, it will be handed off to the operating system. To further enhance the superior reliability of HP Integrity servers, the HP-UX MCA Error Recovery feature adds the ability to recover from some of these Machine Check Aborts (MCAs).

<http://dl.acm.org/citation.cfm?id=1057740>

Soft errors are functional failures resulting from the latching of single-event transients (transient voltage fluctuations at a logic node or SETs) caused by high-energy particle strikes or electrical noise. Due to technology scaling and reduced supply voltages, they are expected to increase by several orders of magnitude in logic circuits. Both combinational and sequential logic circuits are expected to be affected. Many different latch designs to prevent soft errors due to particle strikes on

the latch nodes have been proposed. We review these designs and compare them based on their robustness and their power and performance overheads. We also propose new latch designs, the best of which is vulnerable only to a single-event, multiple-upset without any delay overhead and consumes only 40% power of a standard latch. We expect this work will help designers to select latches for applications where soft error is an important design metric.

[http://en.wikipedia.org/wiki/Montecito_\(processor\)](http://en.wikipedia.org/wiki/Montecito_(processor))

Advanced compensation for errors in cache, for reliable operation under mission-critical workloads. This was code-named Pellston technology during development, and has recently been renamed Intel Cache Safe Technology

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